IN THE CLAIMS

What is claimed is:

1. A method, comprising:

forming a contact hole through a first insulating that is self-aligned with respect to a transistor gate having a gate length less than 0.2 microns without forming a contact hole etch stop layer.

2. The method of claim 1, wherein:

forming a contact hole includes reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide.

3. The method of claim 1, wherein:

forming a contact hole includes reactive plasma etching through a first insulating layer compriing silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

4. The method of claim 3, wherein:

the reactive plasma etching includes introducing CHF_3 and $C_2H_2F_4$ into an etch chamber.

5. The method of claim 4, wherein:

the flow rate of CHF_3 is less than ten times the flow rate of $C_2H_2F_4$.

6. The method of claim 5, wherein:

the flow rate of CHF_3 is in the general range of 3-15 standard centimeter cubed per minute (sccm); and

the flow rate of $C_2H_2F_4$ is in the general range of 10-100 sccm.

7. The method of claim 3, wherein:

the reactive plasma etching includes exciting a plasma with a radio frequency power source that supplies power in the general range of 100 to 1000 Watts.

8. The method of claim 3, wherein:

the reactive plasma etching includes an etch time in the general range of 80 to 200 seconds.

9. The method of claim 3, wherein:

the contact hole is formed on a target object that is biased to an absolute value potential in the general range of 100 to 1500 Volts.

10. The method of claim 3, wherein:

the reactive plasma etching pressure is in the general range of 20-100 milliTorrs.

11. The method of claim 3, wherein:

the reactive plasma etching temperature is in the general range of 0-35 °C.

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12. A method, comprising:

etching a contact hole through a first insulating layer comprising doped silicon dioxide that is self-aligned with respect a conductive structure having insulating sidewalls with an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one.

13. The method of claim 12, wherein:

the insulating sidewalls comprise silicon nitride.

14. The method of claim 12, further including:

forming a first insulating layer comprising a high density plasma silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

15. The method of claim 12, further including:

forming the conducting structure over a substrate; and

forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the substrate that is greater than one hundred to one.

16. The method of claim 12, further including:

forming a hard etch mask comprising an insulating material over the first insulating layer; and

forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one.

17. The method of claim 16, wherein:

the hard etch mask comprises silicon dioxide; and

the first insulating layer comprises phosphorous doped silicon dioxide.

18. A method, comprising:

forming a contact hole through an insulating layer between conducting structures separated from one another by less than 0.4 microns and having sidewalls, without forming a protective liner over the conducting structures, wherein the insulating layer comprises silicon dioxide.

19. The method of claim 18, wherein:

the insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight; and

the sidewalls comprise silicon nitride.

20. The method of claim 18, further including:

forming a hard mask comprising substantially undoped silicate glass over the first insulating layer, the hard mask having openings over a contact hole location.